CLAIMS

1. A broadband modulation PLL comprising:

a PLL portion containing a voltage controlled oscillator, a frequency divider for dividing the frequency of an output signal of the voltage controlled oscillator, a phase comparator for comparing the output of the frequency divider with a reference signal, and a loop filter for averaging the output of the phase comparator;

a first modulation input portion for inputting a first modulation signal to a first position of the PLL portion on the basis of input modulation data; and

a second modulation input portion for inputting a second modulation signal to a second position different from the first position of the PLL portion on the basis of the modulation data, wherein the first modulation signal input to the first position of the PLL portion is added with the second modulation signal at the second position, and any one of the first and second modulation input portions inverts the phase of the modulation data and inputs the modulation signal to the PLL potion at the time of a modulation timing adjustment to adjust the modulation timing of the first modulation signal and the second modulation signal.

2. The broadband modulation PLL according to claim 1, wherein any one of the first modulating portion and the second modulating

portion has an inverter for inverting the phase of the modulation data.

3. The broadband modulation PLL according to claim 1 or 2, wherein at least one of the first modulating portion and the second modulating portion has a delay circuit for adjusting the output timing of the modulation signal.

4. The broadband modulation PLL according to any one of claims 1 to 3, wherein the first modulation input portion generates a frequency-dividing ratio of the frequency divider as the first modulation signal and outputs the first modulation signal to the frequency divider, and the second modulation input portion outputs the second modulation signal to the input side of the voltage controlled oscillator.

5. The broadband modulation PLL according to any one of claims 1 to 4, further comprising a timing controller for generating a modulation timing control signal to adjust the modulation timing of the first modulation signal and the second modulation signal.

6. The broadband modulation PLL according to claim 5, wherein the timing controller generates the modulation timing control signal on the basis of the input signal of the voltage controlled oscillator.

7. The broadband modulation PLL according to claim 5, wherein the timing controller generates the modulation timing control signal on the basis of the output signal of the voltage controlled oscillator.

8. The broadband modulation PLL according to claim 5, further comprising:

a measuring unit for demodulating the output signal of the PLL portion and calculating an amplitude value;

an operator for calculating a timing error on the basis of the amplitude value calculated by the measuring unit; and

a storage unit for storing a timing set value for controlling the timing of at least one of the first modulation input portion and the second modulation input portion which is calculated on the basis of the timing error, wherein the first modulation input portion and the second modulation input portion control the modulation timing on the basis of the set value set in the storage portion.

9. A modulation system having the broadband modulation PLL according to any one of claims 1 to 8.

10. A radio communication device having the broadband modulation PLL according to any one of claims 1 to 8.

11. A timing correcting system for a broadband modulation PLL, comprising:

the broadband modulation PLL according to any one of claims 1 to 4; and

a measuring portion for demodulating an output signal of the broadband modulation PLL and calculating an amplitude value, wherein the broadband modulation PLL has an operating portion for calculating the timing error between the first modulation signal and the second modulation signal on the basis of the amplitude value calculated by the measuring portion, and a storage portion for storing a timing set value for controlling the modulation timing of at least one of the first modulation input portion and the second modulation input portion which is calculated on the basis of the timing error.

12. A timing correcting system for a broadband modulation PLL, comprising:

a broadband modulation PLL;

a measuring portion for demodulating an output signal of the broadband modulation PLL and detecting a value indicating modulation precision; and

a measuring unit for demodulating an output signal of the PLL portion and calculating an amplitude value, wherein the broadband modulation PLL comprises a PLL portion containing a voltage controlled oscillator, a frequency divider for dividing

the frequency of an output signal of the voltage controlled oscillator, a phase comparator for comparing the output of the frequency-divider with a reference signal, and a loop filter for averaging the output of the phase comparator, a firs modulation input portion for inputting a first modulation signal to a first position of the PLL portion, a second modulation input portion for inputting a second modulation signal to a second position different from the first position of the PLL portion on the basis of the modulation data, an operating portion for calculating a timing error on the basis of the amplitude value measured by the measuring unit, and a storage portion for storing a timing set value for controlling the output time of at least one of the first modulation input portion and the second modulation input portion which is calculated on the basis of the timing error, thereby adjusting a modulation timing, the first modulation input portion and the second modulation input portion being controlled so that the timing error is corrected on the basis of the timing set value set in the storage portion.

13. A timing error correcting method in broadband modulation PLL comprising:

a step of inputting to different two points in PLL modulation data which are opposite to each other in phase;

a step of adding modulation signals based on the modulation data;

a step of detecting the timing error between the respective modulation signals on the basis of the added modulation signals; and

a step of correcting an output timing of at least one of the two-point modulations input to the PLL on the basis of the detected timing error.

14. An adjusting method of a radio communication device having a broadband modulation PLL for applying modulation to different two points of PLL, comprising:

a step of setting a modulation timing of the broadband modulation PLL, wherein the modulation timing setting step comprises a step of inputting to different two points of PLL modulation data which are opposite in phase to each other, a step of outputting a modulation signal of the broadband modulation PLL on the basis of the modulation data, a step of demodulating the modulation signal of the broadband modulation PLL to achieve an amplitude value, a step of detecting the timing error between the respective modulation signals and setting a timing set value into a storage portion provided to the broadband modulation PLL, and a step of correcting a timing of at least one of the two-point modulations input to the PLL.

15. An adjusting method of a radio communication device having a broadband modulation PLL for applying modulation to different

two points of PLL, comprising:

a step of setting a modulation timing of the broadband modulation PLL, wherein the modulation timing setting step comprises a step of inputting modulation data to different two points of PLL, a step of outputting modulation signals of the broadband modulation PLL on the basis of the modulation data, a step of demodulating a modulation signal of the broadband modulation PLL and detecting a value indicating a modulation degree, a step of detecting the timing error between the respective modulation signals on the basis of a value indicating the modulation precision and setting a timing set value into a storage portion provided to the broadband modulation PLL, and a step of correcting a timing of at least one of the two-point modulations input to the PLL.